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TO: EXAMINER Stacy Whitmore
EXAMINER'S FAX NUMBER (703) 872-9318
ART UNIT 2812
SERIAL NO. 09/602,422

FROM: Peter S. Zawilski

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OCT 08 2002

REGISTRATION NUMBER: 43,305


TECHNOLOGY CENTER 2800

**PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
580 WHITE PLAINS ROAD
TARRYTOWN, NEW YORK 10591
TELEPHONE: (408) 617-4832**

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Comments/Items attached:

Response to Non-Final Office Action dated 14-AUG-2002



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:
Subramanian S. Meiyappan *et al.*
Serial No. 09/602,422
Filed: June 23, 2000
For: Computer System and Method to Dynamically
Generate System on a Chip Description Files and
Verification Information

Group: 2812
Examiner: Stacy Whitmore
Docket No.: US008612
(Old Docket No. VLSI-3505)

RESPONSE TO AUGUST 14, 2002 OFFICE ACTION

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Assistant Commissioner for Patents
Washington, DC 20231

UUT U 8 2002

Sir:

TECHNOLOGY CENTER 2800

In response to the Office Action dated August 14, 2002, please consider the following amendments and remarks. Note that the Docket No. has been changed per Change of Correspondence Address/Power of Attorney documents filed on March 18, 2002.

In the Claims

Please cancel claim 7 without prejudice. Please replace the claims as shown. Appendix A indicates the changes made to the claims. Appendix B lists the remaining pending claims are shown in clean form.

1. (*Amended*) A System on a Chip (SoC) netlist builder and verification computer system comprising:

a user interface module for providing user friendly and convenient interfaces that facilitate easy entry and modification of user selections and parameters;

an expert system module for analyzing information supplied by said user module and automatically providing SoC building and verification data to a parameter application module;

a parameter application module for applying parameters and developing command line strings based upon information received from said user interface and said expert system;

a chip level netlist generation module for automatically generating a chip level

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